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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,162	08/09/2001	Jordan C. Cookman	ESST-00301	5331

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EXAMINER	
JONES, PRENELL P	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,162	Applicant(s) COOKMAN ET AL.	
	Examiner Prenell P Jones	Art Unit 2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-13 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-13 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1, 5, 13 and 18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U.S. Patent No. 6,327,249. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1, 5, 13 and 18 of the present application merely broadens the scope of the claims 1 and 2 of the Patent by eliminating the elements and their functions of the claims. It has been held that the omission an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also

note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 4, 5, 7, 9-13, 15-18, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sridhar et al in view of Manning et al.

Regarding claims 1, 4, 5, 7, 9-13, 15-18, 21 and 23, Sridhar discloses (Abstract, interfacing between a communication channel and a processor modem (host signal processor/HSP) with software application whereby interrupt signals are generated to indicate the presence and absence of data, (Fig. 3, col. 6, line 26-63) and the architecture includes a CODEC (data

transfer system) that samples incoming signals and transfers data samples to a processor, whereby the samples are eventually transferred to multiple FIFO buffers for storage, buffers consisting of transmit buffer and receive buffer, (col. 7, line 2-59) updating access to buffers as associated with capacity, (col. 5, line 38-55) which are contained in the processor. Sridhar further teaches (col. 6, line 48-57, col. 12, line 14-17) that the processor responds (acknowledge) interrupt signals, (col. 13, line 35-60, col. 15, line 45 thru col. 16, line 23) data samples periodically sent from CODEC, sampling clock wherein the sample data are associated with symbol rate per interrupt, interrupt signals are generate with respect to the monitoring of data samples stored in memory, (Fig. 7, col. 12, line 14-17, col. 15, line 1-35) processor sends interrupt (poll) FIFO (counter) of available data, a no indication (null signal) is recognized when data is not available, (col. 16, line 9-23) transmission and reception associated with buffer storage occurs simultaneously. It is inherent that there is some counting (col. 9, line 54 thru col. 51) associated with the buffers of Sridhar's teachings because the threshold or data capacity of the buffer is monitored for overrun. However, Sridhar is silent on a counter incrementing and decrementing for each data sample transmitted from the circular buffer (FIFO buffer). In analogous art, Manning discloses (Abstract, Figs. 5A, 5B, 6A, 6B, col. 6, line 1-20) efficient utilization of receiver buffers with the implementation of flow control, wherein the architecture consist of plurality of buffer counters that are configured for incrementing buffer when cell is deposited in buffer and decrementing buffer when cells are released from buffer, (col. 10, line 5-61) counter equals or exceeds threshold an update count is recorded (counts beyond range). Manning further discloses (col. 11, line 49-67) incrementing and decrementing logic for all counters, such as, some counters are reset to zero and count down to zero, and adjustment for counter limits are accommodate non-zero counts. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement incrementing

and decrementing each data sample associated with data transfer/data storage of samples with respect to buffer storage as taught in Manning's method and apparatus of sharing buffers with the teachings of Sridhar for the purpose of better managing the utilization of buffer storage.

4. Claims 2, 3, 8, 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sridhar et al as applied to claims 1, 4, 5, 7, 9-13, 15-18, 21 and 23 above, and further in view of Yeh et al (US Pat. 5,721,830).

Regarding claims 2, 3, 8, 19, 20 and 22, as indicated above, Sridhar discloses (Abstract, interfacing between a communication channel and a processor modem (host signal processor/HSP) with software application whereby interrupt signals are generated to indicate the presence and absence of data, (Fig. 3, col. 6, line 26-63) and the architecture includes a CODEC (data transfer system) that samples incoming signals and transfers data samples to a processor, whereby the samples are eventually transferred to multiple FIFO buffers for storage, buffers consisting of transmit buffer and receive buffer, (col. 7, line 2-59) updating access to buffers as associated with capacity, (col. 5, line 38-55) which are contained in the processor. Sridhar further teaches (col. 6, line 48-57, col. 12, line 14-17) that the processor responds (acknowledge) interrupt signals, (col. 13, line 35-60, col. 15, line 45 thru col. 16, line 23) data samples periodically sent from CODEC, sampling clock wherein the sample data are associated with symbol rate per interrupt, interrupt signals are generate with respect to the monitoring of data samples stored in memory, (col. 16, line 9-23) transmission and reception associated with buffer storage occurs simultaneously. It is inherent that there is some counting (col. 9, line 54 thru col. 51) associated with Sridhar's teachings because the threshold or data capacity is monitored for overrun, and Manning discloses (Abstract, Figs. 5A, 5B, 6A, 6B, col. 6, line 1-20)

efficient utilization of receiver buffers with the implementation of flow control, wherein the architecture consist of plurality of buffer counters that are configured for incrementing buffer when cell is deposited in buffer and decrementing buffer when cells are released from buffer, (col. 10, line 5-61) counter equals or exceeds threshold an update count is recorded (counts beyond range). Both Sridhar and Manning are silent on counter has a programmable threshold and generates an interrupt when counter passes threshold and a counter generating interrupts after host responds to first interrupt. In analogous art, Yeh (US Pat 5,721,830) discloses (col. 2, line 33-64) a host signal processing communication system (HSP), which includes circular buffers, and that interfaces with a communication device (CODEC), (col. 4, line 20-65) HSP generates data samples as associated with the DA-AD conversions via a bus to communication device, data samples are transmitted to circular buffer, (col. 3, line 13-16, col. 10, line 26-50) host responds (acknowledges) to interrupt signal, (col. 10, line 38-50) after host responds to an interrupt, a next interrupt is generated, (col. 10, line 11-37) a TMOUT (interrupt) signal is generated to indicate an overflow (programmable threshold) of counter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a counter with programmable threshold feature, as well as, a counter generating interrupts after a host processor responds to a first interrupt as taught by Yeh with the combined teachings of Srihdar and Manning for the purpose of further managing data flow and storage and enhancing storage utilization in a shared communication system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

April 4, 2005

CHI PHAM
SUPERVISORY PATENT EXAMINER
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4/4/05